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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,492	04/21/2004	Sadami Takeoka	60188-820	5291

7590 09/20/2005

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,492	TAKEOKA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) *17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,14 and 15* is/are rejected.

7)☒ Claim(s) *13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/187,269.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 and 11-30 have been cancelled in accordance with Applicant's transmittal letter instructions dated 4/21/04.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 11-16 in the Paper filed 08/29/05 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 4/21/04 is acceptable.

Drawings

4. The formal drawings filed on 4/21/04 are acceptable.

Priority

5. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/187,269, filed on 07/02/2002.

Information Disclosure Statement

6. If applicant is aware of any relevant prior art, he/she requested to cite it on form **PTO-1449** in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11,12,14, and 15 rejected under 35 U.S.C. 102(b) as being anticipated by YAMAMURA (5,341,096).

With regard to claims 11 and 12 Yamamura discloses a semiconductor device comprising a semiconductor wiring substrate 6 having a wiring layer 5; a plurality of chip IPs 1A, 1B mounted on said semiconductor wiring substrate 6 by being bonded thereto; a boundary scan test circuit 7b provided in each of said chip IPs 1A, 1B; and an internal scan chain 7a for an internal scan test, said scan chain being formed in each of said chip IPs 1A,

1B and capable of operating simultaneously with said boundary scan test circuit 7b, wherein at least one of scanning signal input terminals connected to said internal scan chain 7a is a terminal specially formed separately from said boundary scan test circuit 7b. Note figures 2-5, 9, 12A, column 2 lines 11-21, and column 5 lines 11-57 of Yamamura.

With regard to claims 14 and 15 Yamamura discloses a semiconductor device comprising a semiconductor wiring substrate 6 having a wiring layer 5; a plurality of chip IPs 1A, 1B mounted on said semiconductor wiring substrate 6 by being bonded thereto; a boundary scan test circuit 7a provided in each of said chip IPs 1A, 1B; and at least two pieces of wiring Sdin and SDout formed in the wiring layer 5 of said semiconductor wiring substrate 6 to be used only for testing; and an input terminal TBI and an output terminal TAK for a boundary scan test 7a connected to said boundary scan test circuit 7a in each of said chip IP and respectively connected to said two pieces or wiring for testing only, and said boundary scan test circuit 7a in said plurality of chip IPs 1A, 1B is formed so as to also function as an internal scan test circuit 7a in said chip IPs 1A, 1B: wherein an input-side wiring branch SDin and an output-side wiring branch SDout which respectively branch off from an input-side end portion and an output-side end portion of said boundary scan test circuit 7a are formed in each of said chip IPs 1A, 1B; wherein a scan-in terminal through which an internal scan test signal is input is connected to said input-side wiring branch SDin; wherein a scan-out terminal through which a scan test result is output is connected to said output-side wiring branch SDout; and wherein an

input to said in-chip chain can be selected from a signal in said boundary scan test circuit 7a and a signal from said wiring branch. Note figures 2-5, 9, 12A, column 2 lines 11-21, and column 5 lines 11-57 of Yamamura.

Allowable Subject Matter

9. Claims 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

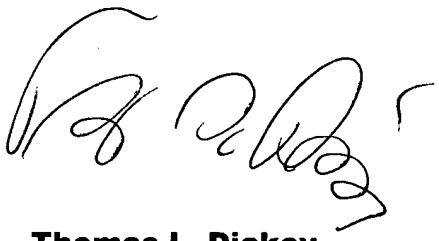
Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
09/05